

## Claims

We claim:

1. 1. An electronic structure, comprising:
  - 2 a semiconductor substrate having a first electrically conductive pad thereon;
  - 3 an organic substrate having a second electrically conductive pad thereon, wherein a
  - 4 surface area of the first pad exceeds a surface area of the second pad; and
  - 5 a solder member electrically coupling the first pad to the second pad.
- 10 2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the
- 20 organic substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.
- 1 3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is  
2 defined as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member,  
3 wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the  
4 semiconductor substrate.
- 1 4. The electronic structure of claim 1, wherein the organic substrate includes an organic material  
2 selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and  
3 combinations thereof.

1       5. The electronic structure of claim 1, wherein the solder member includes a controlled collapse  
2       chip connection (C4) solder ball.

*and  
cont*  
1       6. The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

1 7. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad;

5 a solder member electrically coupling the first pad to the second pad; and

6 an underfill material between the semiconductor substrate and the organic substrate,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

*Surf. Area  
Exceeds  
Pad  
Size*

1       8. An electronic structure, comprising:

2            a semiconductor chip having a first electrically conductive pad thereon;

3            an organic chip carrier having a second electrically conductive pad thereon, wherein a

4            surface area of the first pad exceeds a surface area of the second pad;

5            a solder member electrically coupling the first pad to the second pad; and

6            an underfill material between the semiconductor chip and the organic chip carrier,

7            wherein the underfill material encapsulates the solder member, and wherein the underfill material

8            has an elastic modulus of at least about 1 gigapascal.

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1 9. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad by a factor of at least about

5 1.2; and

6 a solder member electrically coupling the first pad to the second pad.

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1 10. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad by a factor between about

5 1.1 and about 1.3; and

6 a solder member electrically coupling the first pad to the second pad.

100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

1 11. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad by a factor between about

5 1.3 and about 2.0; and

6 a solder member electrically coupling the first pad to the second pad.

1 12. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon; and

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm.

13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the

14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P

15 is defined as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder

16 member, wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the

17 semiconductor substrate.

18. The electronic structure of claim 12, wherein the organic substrate includes an organic

19 material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene,

20 and combinations thereof.

21. The electronic structure of claim 12, wherein the solder member includes a controlled

22 collapse chip connection (C4) solder ball.

17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

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1 18. An electronic structure, comprising:

2 a semiconductor chip having a first electrically conductive pad thereon;

3 an organic chip carrier having a second electrically conductive pad thereon;

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm; and

7 an underfill material between the semiconductor chip and the organic chip carrier,

8 wherein the underfill material encapsulates the solder member, and wherein the underfill material

9 has an elastic modulus of at least about 1 gigapascal.

1 19. An electronic structure, comprising:  
2 a semiconductor substrate having a first electrically conductive pad thereon;  
3 an organic substrate having a second electrically conductive pad thereon;  
4 a solder member electrically coupling the first pad to the second pad, wherein a  
5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor  
6 substrate is at least about 0.25 mm; and  
7 an underfill material between the semiconductor substrate and the organic substrate,  
8 wherein the underfill material encapsulates the solder member, and wherein the underfill material  
9 has an elastic modulus of at least about 1 gigapascal.

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1 20. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon; and

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.40 mm.



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1 21. A method of forming an electronic structure, comprising:  
2 forming a semiconductor substrate having a first electrically conductive pad thereon;  
3 forming an organic substrate having a second electrically conductive pad thereon,  
4 wherein a surface area of the first pad exceeds a surface area of the second pad; and  
5 electrically coupling, by use of a solder member, the first pad to the second pad.

1 22. The method of claim 21, wherein a coefficient of thermal expansion (CTE) of the organic  
2 substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.

1 23. The method of claim 21, wherein P is between about .15 and about .75, wherein P is defined  
2 as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member,  
3 wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the  
4 semiconductor substrate.

1 24. The method of claim 21, wherein the organic substrate includes an organic material selected  
2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations  
3 thereof.

1 25. The method of claim 21, wherein the solder member includes a controlled collapse chip  
2 connection (C4) solder ball.

1 26. The method of claim 21, wherein the solder member includes a lead-tin alloy.

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1 27. A method of forming an electronic structure, comprising:

2 forming a semiconductor chip having a first electrically conductive pad thereon;

3 forming an organic chip carrier having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad;

5 electrically coupling, by use of a solder member, the first pad to the second pad; and

6 placing an underfill material between the semiconductor chip and the organic chip carrier,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

1       28. A method of forming an electronic structure, comprising:

2           forming a semiconductor substrate having a first electrically conductive pad thereon;

3           forming an organic substrate having a second electrically conductive pad thereon,

4        wherein a surface area of the first pad exceeds a surface area of the second pad;

5           electrically coupling, by use of a solder member, the first pad to the second pad; and

6           placing an underfill material between the semiconductor substrate and the organic

7        substrate, wherein the underfill material encapsulates the solder member, and wherein the

8        underfill material has an elastic modulus of at least about 1 gigapascal.

1 29. A method of forming an structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at

5 least about 1.2; and

6 electrically coupling, by use of a solder member, the first pad to the second pad.

1       30. A method of forming an electronic structure, comprising:

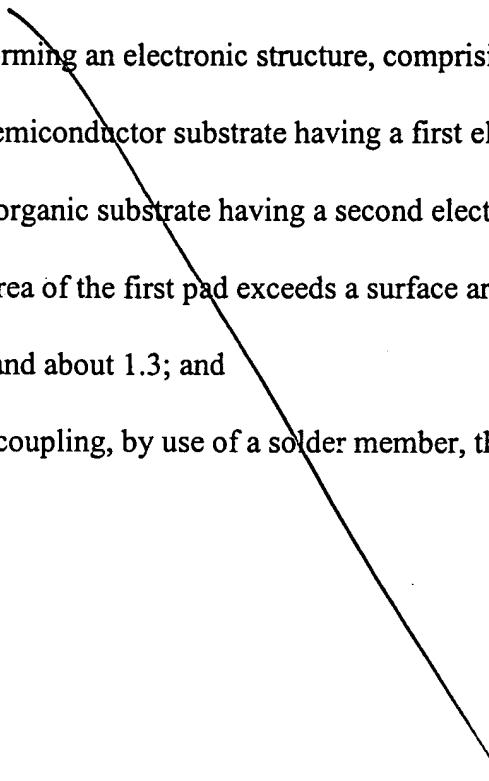
2           forming a semiconductor substrate having a first electrically conductive pad thereon;

3           forming an organic substrate having a second electrically conductive pad thereon,

4       wherein a surface area of the first pad exceeds a surface area of the second pad by a factor

5       between about 1.1 and about 1.3; and

6           electrically coupling, by use of a solder member, the first pad to the second pad.



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1      31. A method of forming an electronic structure, comprising:

2              forming a semiconductor substrate having a first electrically conductive pad thereon;

3              forming an organic substrate having a second electrically conductive pad thereon,

4              wherein a surface area of the first pad exceeds a surface area of the second pad by a factor

5              between about 1.3 and about 2.0; and

6              electrically coupling, by use of a solder member, the first pad to the second pad.

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1 32. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon; and

4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein

5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm.

1 33. The method of claim 32, wherein a coefficient of thermal expansion (CTE) of the organic

2 substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.

1 34. The method of claim 32, wherein R is between about .15 and about .75, wherein P is defined

2 as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member,

3 wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the

4 semiconductor substrate.

1 35. The method of claim 32, wherein the organic substrate includes an organic material selected

2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations

3 thereof.

1 36. The method of claim 32, wherein the solder member includes a controlled collapse chip

2 connection (C4) solder ball.

1 37. The method of claim 32, wherein the solder member includes a lead-tin alloy.

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1       38. A method of forming an electronic structure, comprising:

2           forming a semiconductor chip having a first electrically conductive pad thereon;

3           forming an organic chip carrier having a second electrically conductive pad thereon;

4           electrically coupling, by use of a solder member, the first pad to the second pad, wherein

5       a distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6       substrate is at least about 0.25 mm; and

7           placing an underfill material between the semiconductor chip and the organic chip carrier,

8           wherein the underfill material encapsulates the solder member, and wherein the underfill material

9       has an elastic modulus of at least about 1 gigapascal.

1       39. A method of forming an electronic structure, comprising:

2           forming a semiconductor substrate having a first electrically conductive pad thereon;

3           forming an organic substrate having a second electrically conductive pad thereon;

4           electrically coupling, by use of a solder member, the first pad to the second pad, wherein

5       a distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6       substrate is at least about 0.25 mm; and

7           placing an underfill material between the semiconductor substrate and the organic

8       substrate, wherein the underfill material encapsulates the solder member, and wherein the

9       underfill material has an elastic modulus of at least about 1 gigapascal.

1 40. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon; and

4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein

5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.40 mm.

*1st claimed*

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